other. The Examiner further rejected claims 1-3, 5-15, 17-18 and 38-45 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,169,328 to Mitchell ("Mitchell") in view of U.S. Patent No. 5,960,260 to Umehara ("Umehara"). Applicant disagrees with these grounds of rejection and wishes to clarify various distinctions of Applicant's invention over the cited art. Reconsideration of the invention is therefore requested in light of the present amendment and following remarks.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions as they are discussed.

The various embodiments of the present invention are directed to a semiconductor package assembly having a plurality of pieces of a compliant adhesive film to adhere a BGA-type semiconductor die to an organic substrate or polyimide substrate interposer. The compliant adhesive film reduces failures in semiconductor package solder bonds by reducing undesired shear stresses that may result from unmatched coefficients of thermal expansion for the interposer and the semiconductor die. A further advantage associated with the various embodiments of the invention is that the cumulative thermal expansion for multiple strips of adhesive film is less than the thermal expansion for a single layer of an elastomeric film. As a consequence, the stress on the BGA-package wire bond joints resulting from the different coefficients of thermal expansion between the die and the substrate are reduced.

In one particular embodiment, as described at page 8, lines 10-20, and further shown in Figure 2B of the present application, the compliant adhesive film may include one or more carrier layers having adhesive layers disposed on opposing exterior surfaces of the carrier layers. The carrier layers thus described advantageously permit the adhesive material to be positioned on the carrier layers before the adhesive layers are presented to the die and the interposer.

The Examiner has cited the Umehara reference for disclosing a semiconductor package having a plurality of compliant adhesive strips disposed between a mounting surface and a semiconductor die that extend along one dimension of the package. Umehara does not

disclose a carrier layer having adhesive layers disposed on opposing surfaces of the carrier layer. Instead, and with reference now to Figures 6A-14, Umehara discloses a polyimide thermoplastic layer 84 and an adhesive layer 92 positioned on a base film 90 in alternating strips to form a dicing tape 102, as shown in Figures 6A-6C. The dicing tape 102 is then positioned against the wafer 63 as shown in Figure 7, where the adhesive layer 92 adheres to the wafer 63, while the polyimide thermoplastic layer 84 provides no adhesion to the wafer 63 (see col. 16, lines 35-41). The wafer 63 may then be diced, as shown in Figures 7 and 8, with the adhesive layer 92 fixedly holding the wafer 63 in place. The resulting structure is subjected to ultraviolet (UV) radiation 65 from a UV source, as shown in Figure 9. The UV radiation 65 photocures the adhesive layer 92 *so that the IC chip 10 and the adhesive 92 may be easily peeled apart* as described at col. 16, line 50-55, and as further shown in Figures 11A and 11B. Referring now to Figure 12, the chip 10 and the tape 90 are separated , with the polyimide thermoplastic layer 84 now adhering to the chip 10. Figure 14 shows the chip 10 being joined to the mounting pad 81 through the application of heat and pressure.

Accordingly, the applicant respectfully asserts that the Umehara reference fails to teach a carrier layer having one or more layers and having an adhesive layer on opposing exterior surfaces of the one or more carrier layers. Assuming, *arguendo*, the base film 90 (shown in Figures 6-12 of the Umehara reference) constitutes the carrier layer, applicant would particularly point out that *the carrier would be completely removed from the structure, so that no carrier would remain at the conclusion of the disclosed process.*

The Examiner has also cited the Mitchell reference for disclosing a flexible organic interposer. The Mitchell reference, however, also fails to disclose carrier layer having one or more layers and having an adhesive layer on opposing exterior surfaces of the one or more carrier layers.

Turning now to the claims, patentable differences between the claims and the applied art will be specifically pointed out. Claim 1, as amended, recites in pertinent part, "A semiconductor device package, comprising...a semiconductor die...at least one electrically conductive external terminal...an interposer having a die attach surface and an external surface opposite of the die attach surface...and a plurality of elongated strips of compliant adhesive film, *... the strips further including a compliant carrier layer having a pair of opposing surfaces with*

a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die." (Emphasis added). Umehara does not disclose or suggest this. Instead, Umehara discloses forming a tape having alternating strips of a polyimide thermoplastic material and an adhesive material. The resulting structure is applied to the die with the adhesive bonding to the die. The adhesive is cured and physically separated from the die to leave only the polyimide layer remaining.

Claim 11, as amended, recites in pertinent part, "A device package assembly for a semiconductor die...comprising [the process]...laminating a plurality of strips of compliant adhesive film to an interposer...attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated...*the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die*; and bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad. (Emphasis added). Again, Umehara does not disclose or suggest this, as explained more fully above.

Claim 38, as amended, recites in pertinent part, "A semiconductor device package, comprising...a semiconductor die...an interposer having a die attach surface...and a plurality of elongated strips of compliant adhesive film...*the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.*" (Emphasis added). Umehara does not disclose or suggest this, as previously explained. Moreover, the Mitchell reference does not provide the missing disclosure.

Finally, claim 42, as amended, recites in pertinent part, "A semiconductor device package, comprising...a semiconductor die...an interposer having a die attach surface...and a

plurality of elongated strips of compliant adhesive film...*including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.* (Emphasis added). Umehara does not disclose or suggest this, as previously explained. And again, the Mitchell reference does not provide the missing disclosure.

Accordingly, claims 1, 11, 38 and 42 are now allowable over the cited references. Further, claims that depend from claims 1, 11, 38 and 42 are similarly allowable in view of the allowability of the base claim and further in view of the additional limitations present in the dependent claims.

The Examiner has further rejected claims 10 and 44 under 35 U.S.C. § 112, first paragraph, claiming that the specification "...does not reasonably provide for strips positioned at right angles...". The applicant respectfully disagrees, and directs the Examiner to page 7, lines 15-20, where it is stated that: "...each of the single strips may be separated into multiple pieces arranged along the length of the die. *Alternatively, the pieces of adhesive film 20a-c may also be arranged at right angles near the corners of the die 12*, or oriented to extend across the width of the die 12." (Emphasis added).

The Examiner further asserts that claims 10 and 44 are in contradiction to independent claims 1 and 42. Accordingly, claims 1 and 42 have been amended to recite that each strip is elongated, and has a first length and a second length perpendicular to the first length, with the first length being substantially greater than the second length, and have further omitted the contradictory claim language, as indicated.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Steven H. Arterberry
Registration No. 46,314

SHA:sj

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Three Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of opposed lateral edges;

at least one electrically conductive external terminal;

an interposer having a die attach surface and an external surface opposite of the die attach surface disposed in between the semiconductor die and the at least one external terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed [in] between the semiconductor die and the interposer [to adhere the semiconductor die to the die attach surface of the interposer,] the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die. [the strips of compliant adhesive film each extending substantially less than the distance between the second pair of opposed lateral edges.]

11. (Three Times Amended) A device package assembly for a semiconductor die being constructed from a process comprising:

laminating a plurality of strips of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer being formed of an organic

substrate or a polyimide substrate and further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges, [the strips each extending substantially less than the distance between the second pair of opposed lateral edges] the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

38. (Twice Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die [to adhere the semiconductor die to the die attach surface of the interposer,] the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the

semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die. [the strips of compliant adhesive film each extending substantially less than the distance between the second pair of opposed lateral edges.]

42. (Three Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer, the strips of compliant adhesive film further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die. [each extending substantially less than the distance between the second pair of opposed lateral edges.]